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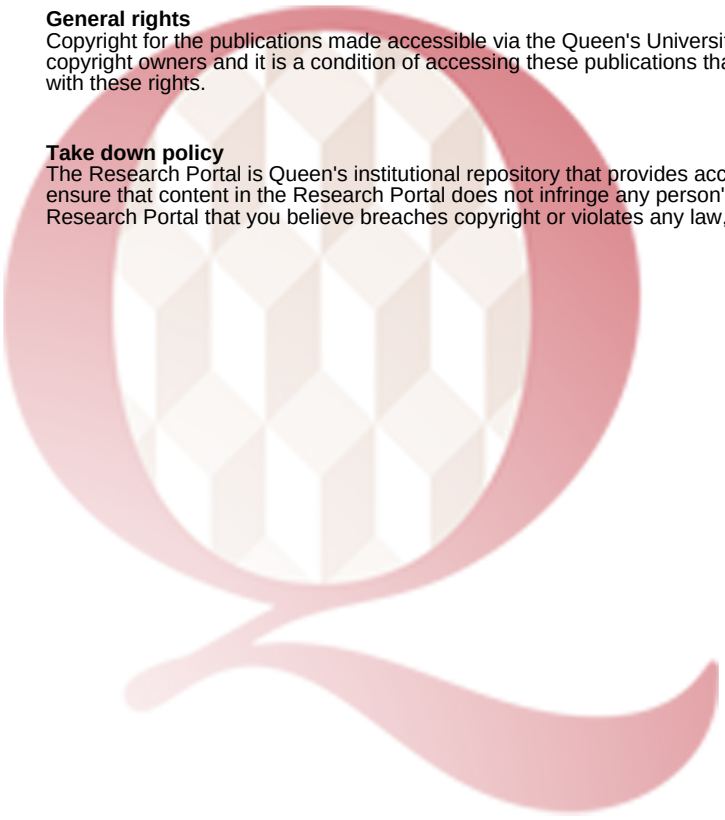

Holistic Design Strategy for High-Selectivity Low-Loss Integrated Millimetre-Wave Image-Reject Filters

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Abstract: To alleviate practical limitations in the design of mm-wave on-chip image-reject filters, systematic design methodologies are presented. Three low-order filters with high-selectivity and low-loss characteristics are designed and compared. Transmission zeroes are created by means of a quarter-wave transmission line (filter 1) and a series LC resonator (filters 2 and 3). Implemented on SiGe, the filters occupy 0.125, 0.064, and 0.079 mm^2 chip area including pads. The measured transmission losses across 81-86 GHz E-Band frequency range are 3.6-5.2 dB for filter 1, 3.1-4.7 dB for filter 2 and 3.6-5 dB for filter 3 where rejection levels at the image band are greater than 30 dB.

Key words: Dispersion; E-band; image-reject filter; MMIC; mm-wave; quality factor; SiGe; transmission line; transmission zero.

1. Introduction

Overcrowded spectra of low-GHz wireless systems such as Wi-Fi and WiMAX and increased demand for high data-rate wireless transmission have recently been fuelling the development of 71-76 GHz and 81-86 GHz E-band systems, [1]-[4]. E-band systems offer a fresh opportunity to establish fiber-like high-speed wireless links with full duplex throughput of 1 Gbps or above. Unlike the 60-GHz band, E-band is not penalized by the transmission loss due to oxygen absorption and is therefore suited for long-distance backhaul point-to-point communications [5]. In addition, the availability of generous bandwidth within E-band enables deployment of low-complexity modulation schemes such as OOK and BPSK. Furthermore, since the wavelengths of millimeter-wave (mmW) signals are extremely small (1-10 mm) the large numbers of antennas essentially required to provide high gain and to enable beamforming can be conveniently made in a physically small form factor.

In the E-band heterodyne receiver, Fig. 1, employing a frequency quadrupler (N = 4) and a divide-by-two frequency divider (M = 2), the calculated LO and IF frequencies are respectively $8/9\times f_{RF}$ and $1/9\times f_{RF}$. As a result, the receiver image frequency will be located at $7/9\times f_{RF}$ corresponding to 63-66.9 GHz for f_{RF} = 81-86 GHz i.e. upper E-band. Such heterodyne architectures typically require high image noise rejection of at least 30 dB so that overall system noise figure can be kept low. A simple notch filter typically incorporated within the LNA–Mixer circuits, [6], can only provide a modest image rejection of around 10-15 dB.

Waveguide-type filters typically have low insertion loss and high selectivity but they are bulky. On the other hand, on-chip planar filters [7]-[20] offer more compact solution but they are lossy particularly when realised in low resistivity substrate technology. For example, in [21], a third-order bandpass filter designed at 9.45 GHz

and realised in 130 nm CMOS technology exhibited a rather high insertion loss of 15.6 dB. Another major challenge in the design of on-chip filters is that the rejection levels provided by low-order (and thus less lossy) filters at the image frequency are inherently poor. High-order filters can provide high selectivity but require large component counts, leading to large chip area and high loss.

This paper addresses the aforementioned design trade-offs in order to arrive at optimum filter synthesis through deployment of systematic design methodologies for the realization of compact on-chip image-reject filters (IRF) that provide low insertion loss within the 81-86 GHz operating band frequency range, and, at the same time facilitate high rejection levels within the 63-66.9 GHz image band frequency range.

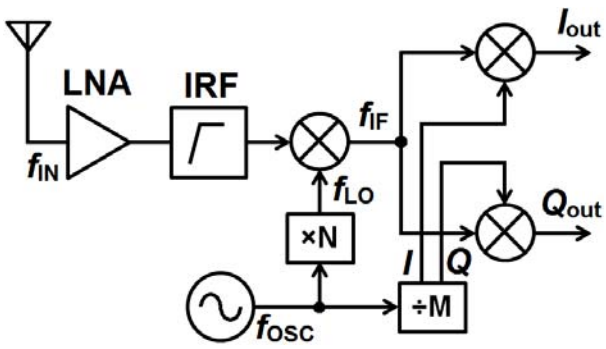


Fig. 1. Heterodyne receiver architecture with a frequency multiplier ×N and a frequency divider ÷M.

2. Filter Synthesis

2.1 Third-Order High Pass Filter with RC Parallel Loading

As a starting point a third-order high-pass filter (HPF) is chosen due to its simplicity. As illustrated in Fig. 2(a), the filter is comprised of a series capacitance $C_X/2$ shunted on both sides by inductance L_X. Source and load impedances are represented by a parallel RC network where R is typically 50 Ω and C represents the parasitic capacitance of input/output pads (C_{pad}) whose effects are detrimental at mmW

frequencies and therefore have to be accounted for in the design. Due to the circuit's symmetry, only a half circuit is analysed. The expression for the intermediate resistance R_I, (1), can be derived from Fig. 2(b). By re-arranging (1) and subsequently setting the real and imaginary parts of the left-hand side equal to the right-hand side, the expressions for L_X (2) and C_X (3) can be obtained wherein $G = 1/R$ and $G_I = 1/R_I$. Notice that L_X is a function of R, C, and R_I whereas C_X is merely a function of R and R_I but not C.

For a pre-determined value C = 25 fF, the values of the shunt inductance L_X and the series capacitance $C_X/2$ are plotted against R_I in Fig. 2(c). As R_I increases, the value of L_X increases. Capacitance $C_X/2$ reaches a minima at R_I = 25 Ω. For a fixed R_I = 25 Ω, the values of L_X and $C_X/2$ are plotted against C in Fig. 2(d). As C increases, the value of L_X decreases. The value of $C_X/2$ is constant regardless of C value. The effects that parameter R_I has on transmission and return losses are illustrated in Figs. 3(a)-(b). Small R_I values result in high rejection level and narrow-band matching. A similar trade-off between out-of-band rejection level and matching bandwidth can also be observed from Figs. 3(c)-(d) where large C yields high rejection level and reduced matching bandwidth.

$$R_I = \frac{1}{\frac{1}{R}+j\omega C+\frac{1}{j\omega L_X}} + \frac{1}{j\omega C_X} \tag{1}$$

$$L_X = \frac{1}{\omega\left\{\omega C+\sqrt{G(G_I-G)}\right\}} \tag{2}$$

$$C_X = \frac{GG_I}{\omega\sqrt{G(G_I-G)}} \tag{3}$$

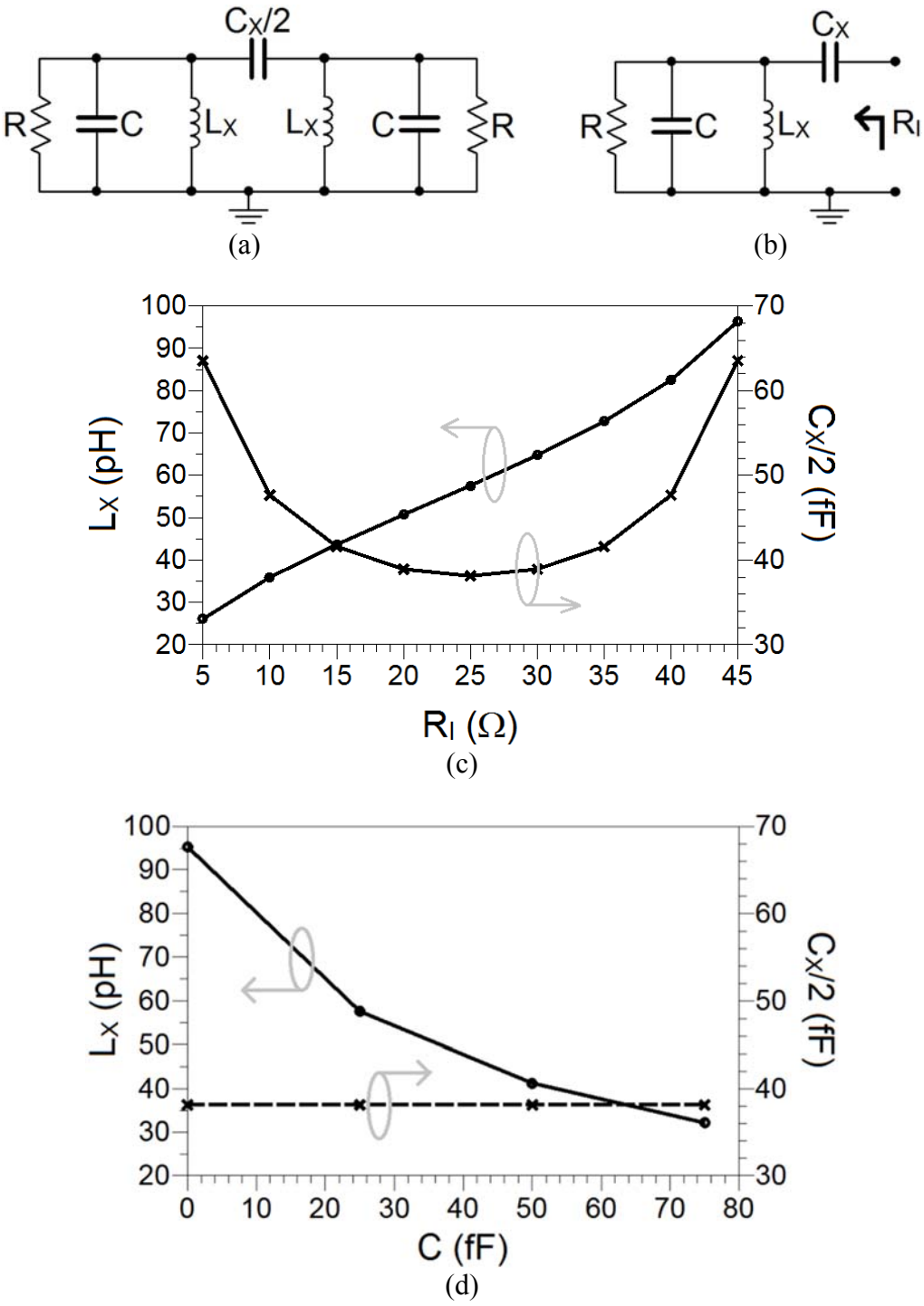
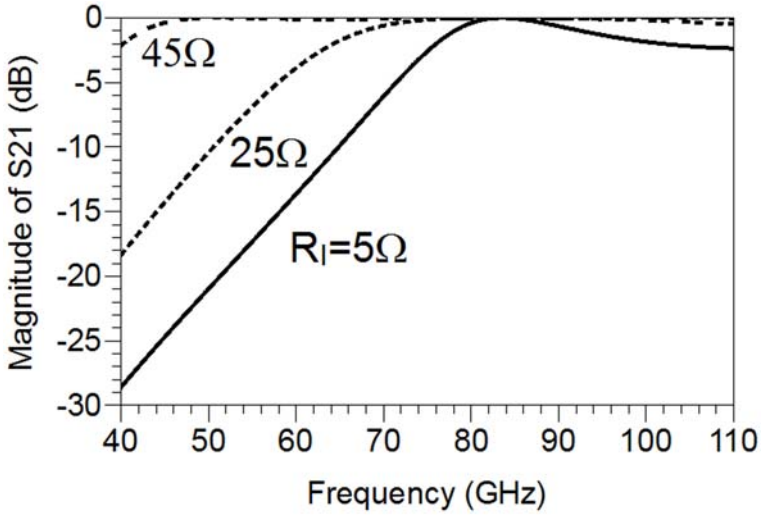
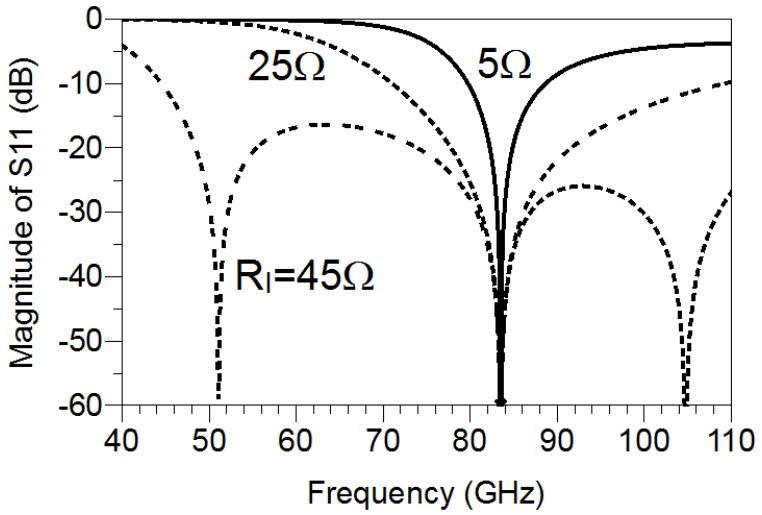


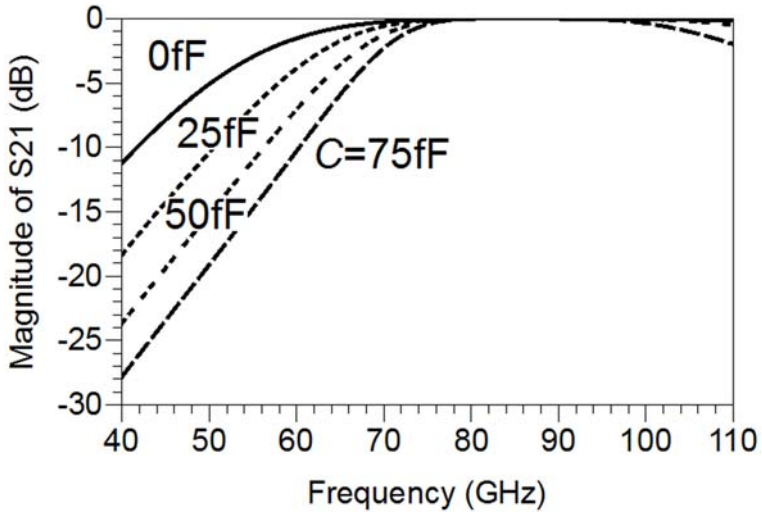
Fig. 2. HPF with RC parallel loading: (a) full-circuit, (b) half-circuit, (c) L_X and C_X as a function of R_I where R = 50 Ω and C = 25 fF, (d) L_X and C_X as a function of C where R = 50 Ω and R_I = 25 Ω.


45Ω
25Ω
RI=5Ω
Magnitude of S21 (dB)
Frequency (GHz)
0
-5
-10
-15
-20
-25
-30
40
50
60
70
80
90
100
110

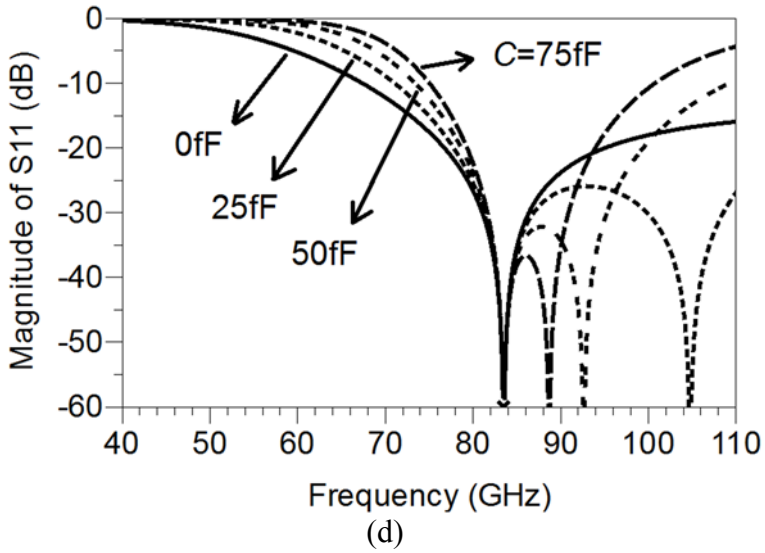
(a)


25Ω
5Ω
RI=45Ω
Magnitude of S11 (dB)
Frequency (GHz)
0
-10
-20
-30
-40
-50
-60
40
50
60
70
80
90
100
110

(b)


0fF
25fF
50fF
C=75fF
Magnitude of S21 (dB)
Frequency (GHz)
0
-5
-10
-15
-20
-25
-30
40
50
60
70
80
90
100
110

(c)



(d)

Fig. 3. (a) & (b) The effect of parameter R_1 on the transmission and return losses of the circuit in Fig. 2(a) where R = 50 Ω and C = 25 fF, (c) & (d) the effect of C on the transmission and return losses of the circuit in Fig. 2(a) where R = 50 Ω and R_1 = 25 Ω.

2.2 High-Selectivity Filter with λ/4 Transmission Line

Low-order filter such as that in Fig. 2(a) cannot provide high selectivity required to adequately reject the image noise. For example, for C = 25 fF and R_1 = 25 Ω, low insertion loss and high return loss across the operating band can be obtained but the attenuation level across the image band is only 3-5 dB, Figs. 3(a)-(b). Increasing the order of the filter can improve the rejection level but this will require a more sophisticated circuit i.e. increased component count and larger chip area.

Consider now Fig. 4(a) where the shunt inductance L_X in Fig. 2(a) is replaced with an open-circuited quarter-wave stub. This stub creates a transmission zero at the image frequency so that high selectivity can be obtained. Suppose $f_1 \approx 65$ GHz i.e. image frequency and f_2 = 83.5 GHz i.e. midpoint of operating band 81-86 GHz. The electrical length of the stub is designed to be 90° (θ_1) at f_1 thus shorting the image noise. At f_2, θ_2 will be larger than 90° (4), and as a result, the stub will behave like an inductance. This inductance must be set equal to L_X (2) in order to retain low insertion loss across the operating band as illustrated in Fig. 3(a). The characteristic impedance

of the stub, Z_0, can be calculated using (5).

$$\theta_2 = \frac{f_2}{f_1}\, 90° \tag{4}$$

$$Z_{in}|_{\omega=\omega_2} = \frac{Z_0}{j \tan\theta_2} = \frac{j\, Z_0}{\tan(180° - \theta_2)} \leftrightarrow j\, \omega_2\, L_X$$

$$\therefore\ Z_0 = \omega_2 L_X \tan(180° - \theta_2) \tag{5}$$

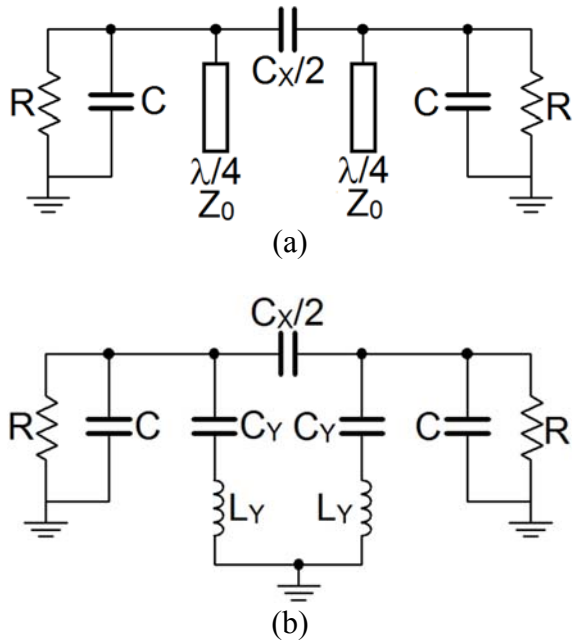


Fig. 4. Circuit schematics of high-selectivity filter employing: (a) λ/4 TL and (b) series LC resonator.

2.3 High-Selectivity Filter with Series LC Resonator

The implementation of the quarter-wave transmission line (TL) employed in Fig. 4(a) consumes a considerable amount of chip area, even at millimetre-wave frequencies. In order to miniaturize the filter in Fig. 4(a) while retaining its low loss and high selectivity characteristics, the λ/4 stub is replaced with a series LC resonator, Fig. 4(b). Transmission zero at the image frequency is created by resonating L_Y with C_Y at f_1 (6). At f_2, this series LC network will present a net inductive reactance whose

value must be set equal to $\omega_2 L_X$ in order to maintain low insertion loss across the operating band. The value of L_Y can be determined using (7).

$$\omega_1^2 L_Y C_Y = 1 \tag{6}$$

$$Z_{LC}|_{\omega=\omega_2} = j\left(\omega_2 L_Y - \frac{1}{\omega_2 C_Y}\right) = j\,\frac{\alpha^2-1}{\alpha^2}\,\omega_2\,L_Y \;\leftrightarrow\; j\,\omega_2\,L_X$$

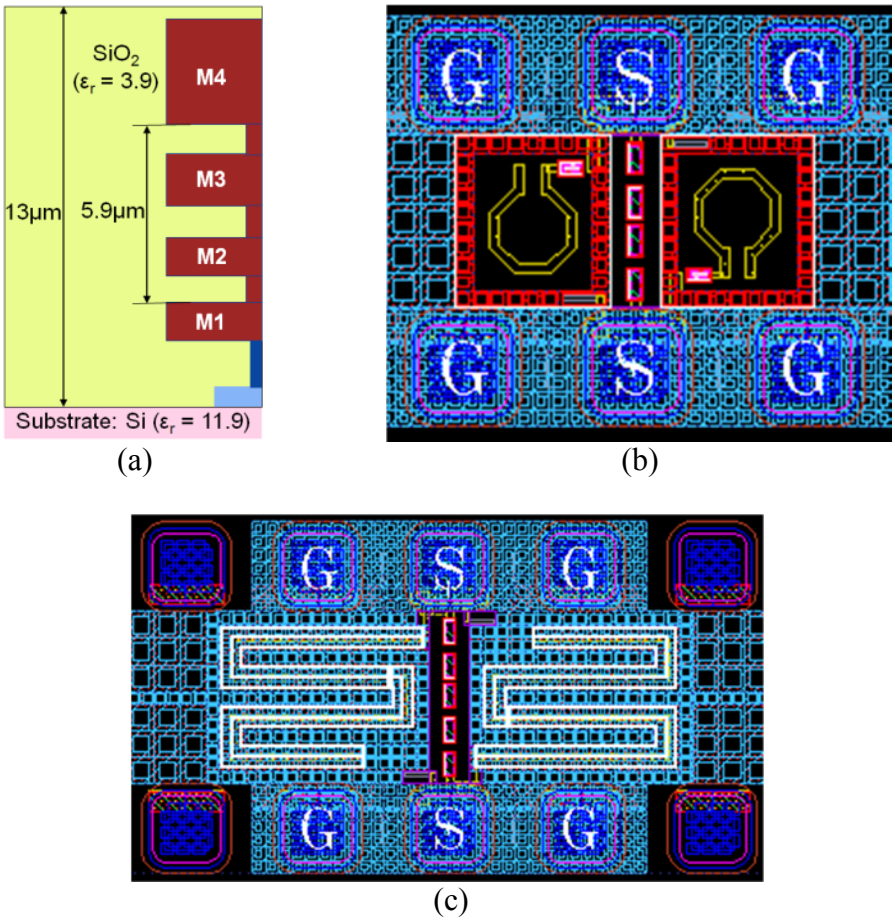
$$\therefore\; L_Y = \frac{\alpha^2}{\alpha^2-1}\,L_X \tag{7}$$

where:

$$\alpha = \omega_2/\omega_1\,,\;\; \alpha > 1 \tag{8}$$

3. Design and Simulation

The image-reject filters were designed using Infineon B7HF200 SiGe technology [22]. In this process, four copper metal layers (M1–M4) can be utilized to realize passive components such as spiral inductors, transformers, and microstrip lines. The cross section of the metal layer stack is shown in Fig. 5(a). The topmost metal, M4, is 2.8-μm thick. Dielectric compounds sandwiched between two metal layers are composed of silicon dioxide (SiO_2) and silicon nitrate (Si_3N_4). The smallest available pad measures 68 μm × 68 μm and it has an equivalent parasitic capacitance (C_{pad}) 25 fF. Metal-insulator-metal (MIM) capacitors are also provided within this process.



(a) (b)

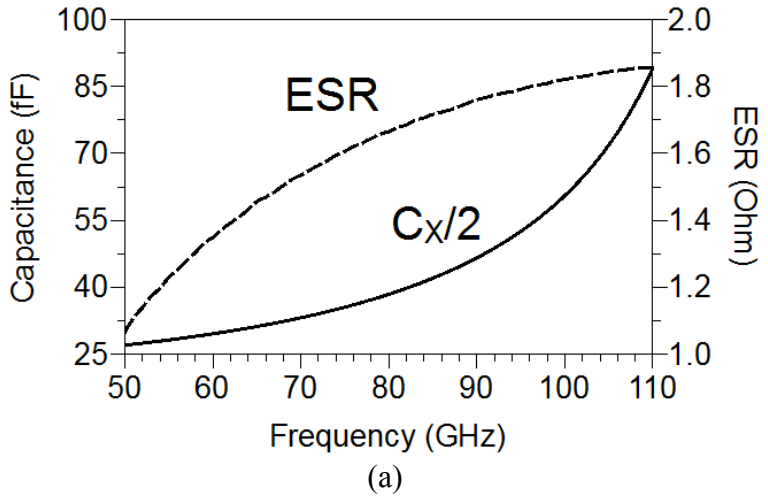
(c)

Fig. 5. (a) Metal layer stack of the Infineon B7HF200 SiGe process
(b) Layout of the series LC resonator filter
(c) Layout of the λ/4 TL filter

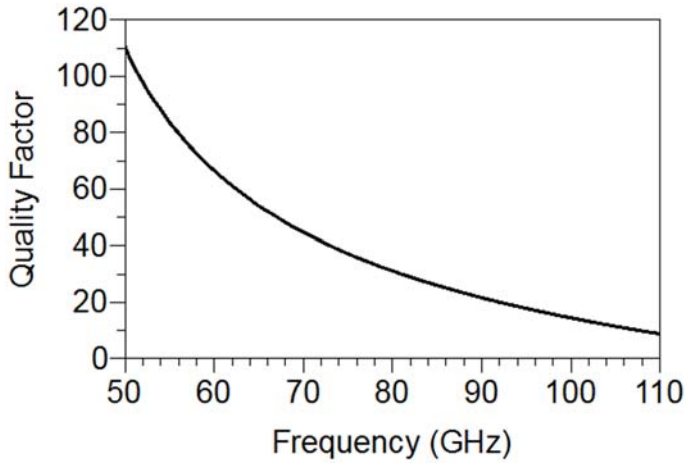
3.1 Design Procedure for the λ/4 TL Filter

For R = 50 Ω, R_I = 20 Ω and $C = C_{pad}$ = 25 fF, the values of $C_X/2$ and L_X in Fig. 2(a) calculated using (2)-(3) are 40 fF and 50 pH, respectively. Capacitance $C_X/2$ was implemented using five 5.6 μm × 15.5 μm MIM capacitors connected in series rather than a single smaller MIM capacitor chiefly because the capacitance variation across the operating band is lower in the former case. Small capacitance variation is required to guarantee low insertion loss across the operating band. On the other hand the impact of capacitance variation across the image band is not critical since the image signal will be shorted by the λ/4 stub, Fig. 4(a). The capacitance value, electrical series resistance (ESR) and quality factor of the MIM capacitor $C_X/2$ simulated in SONNET are plotted

versus frequency in Fig. 6, and their values at 63 GHz, 81 GHz and 86 GHz are presented in Table I.



(a)



(b)

Fig. 6. (a) Capacitance value, parasitic series resistance and (b) quality factor of the MIM capacitor $C_X/2$ simulated in SONNET.

Table I. Capacitance value, parasitic series resistance and quality factor of the MIM capacitor $C_X/2$ simulated in SONNET

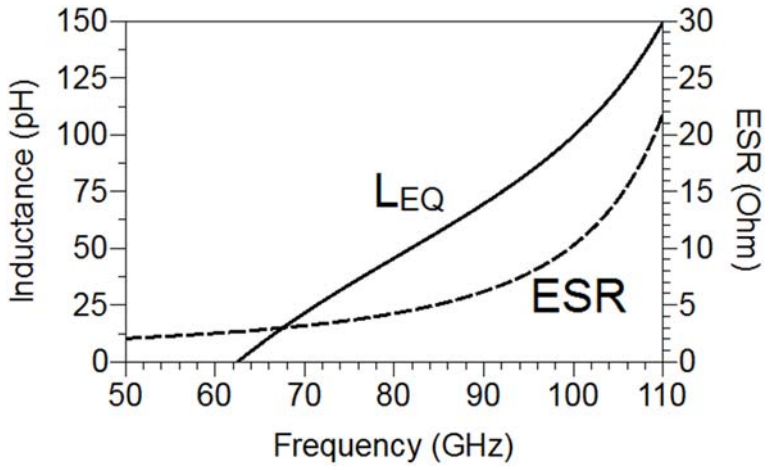
	63 GHz	81 GHz	86 GHz
Capacitance (fF)	30.5	39	43
ESR (Ω)	1.4	1.7	1.7
Quality factor	59	30	25

The physical length of the open-circuit λ/4 stub is initially estimated using:

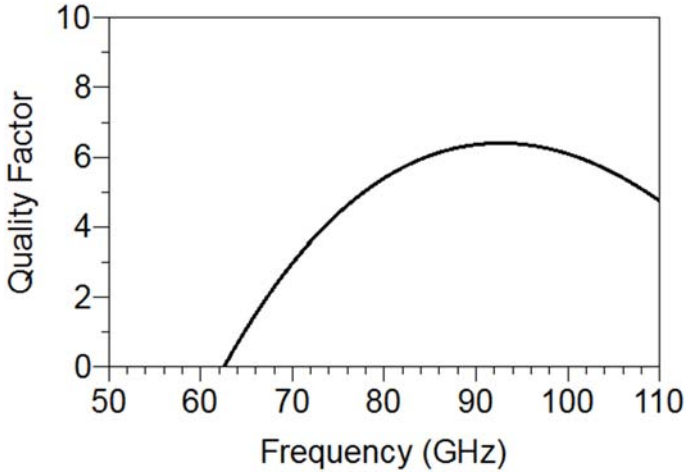
$$l_{\lambda/4} = \frac{c}{4 f_1 \sqrt{\varepsilon_{r\_eff}}} \qquad (9)$$

where c is the speed of light and ε_{r_eff} is the effective relative permittivity of the substrate. Afterwards, it needs to be optimized using electromagnetic (EM) simulator so as the impedance achieved at f_1 is as low as possible. The width of the λ/4 stub is initially calculated using (5) and then meticulously tuned until its net inductance value at f_2 is equal to L_X. The net inductance value, ESR and quality factor of the open-circuit λ/4 stub simulated in SONNET are plotted versus frequency in Fig. 7, and their values at 63 GHz, 81 GHz and 86 GHz are summarised in Table II. The net inductance value of the stub varies by around 25% across the operating band. At 63 GHz, the λ/4 stub transforms an open circuit into a low impedance of 2.7 Ω. Due to low resistivity of the silicon substrate, the quality factor of the stub is rather poor, i.e., less than 7, leading to a high loss. As the frequency increases, the quality factor of the stub tends to increase until it reaches its peak. This trend is in stark contrast with that in Fig. 6(b) where the quality factor of the MIM capacitor degrades rapidly as the frequency increases.

The layout of the λ/4 TL filter is depicted in Fig. 5(c). It measures 468 μm × 266 μm. In order to miniaturize the overall chip size the λ/4 TL was meandered and its effective length was reduced to 600 μm. Adjacent parallel arms are separated relatively far apart at 30 μm in order to reduce EM couplings which are not accounted for in the standard TL model provided by the foundry. The signal line of the TL was realized on M4 with width = 5 μm and the ground plane on M2 with its width set at 3× the signal line width.



(a)



(b)

Fig. 7. (a) Net inductance value, parasitic series resistance and (b) quality factor of the open-circuit λ/4 stub simulated in SONNET.

Table II. Net inductance value, parasitic series resistance and quality factor of the open-circuit λ/4 stub simulated in SONNET

	63 GHz	81 GHz	86 GHz
Inductance (pH)	1.4	48	60
ESR (Ω)	2.7	4.4	5.3
Quality factor	0.2	5.6	6.1

3.2 Design Procedure for the Series LC Resonator Filter

Equation (7) is valid only under assumptions that the inductance values of L_Y at f_1 and f_2 are identical and so are the capacitance values of C_Y at f_1 and f_2. In practice, their values are strongly dependent on frequency, i.e. $L_{Y1} \neq L_{Y2}$ and $C_{Y1} \neq C_{Y2}$ (note

that L_{Y1} and L_{Y2} are the inductance values of L_Y at f_1 and f_2 respectively; C_{Y1} and C_{Y2} are the capacitance values of C_Y at f_1 and f_2). In order to take this practical limitation into account, (6) and (7) must be modified as (10) and (11). Parameters k_L and k_C in (12)-(13) which represent the ratio of the inductance values (L_Y) or the capacitance values (C_Y) at f_1 and f_2 can be adjusted according to the geometries of the spiral inductor and MIM capacitor used in the layout. For example, the values of k_L can be adjusted by varying the metal trace width, the number of turns, and the spacing between two adjacent metal traces of a spiral inductor.

$$\omega_1^2 L_{Y1} C_{Y1} = 1 \qquad (10)$$

$$Z_{LC}|_{\omega=\omega_2} = j\left(\omega_2 L_{Y2} - \frac{1}{\omega_2 C_{Y2}}\right) = j\,\frac{\alpha^2 k_L k_C - 1}{\alpha^2 k_C}\,\omega_2 L_{Y1} \leftrightarrow j\,\omega_2 L_X$$

$$\therefore\ L_{Y1} = \frac{\alpha^2 k_C}{\alpha^2 k_L k_C - 1}\,L_X \qquad (11)$$

where:

$$k_L = L_{Y2}/L_{Y1}\,,\ \ k_L > 1 \qquad (12)$$

$$k_C = C_{Y2}/C_{Y1}\,,\ \ k_C > 1 \qquad (13)$$

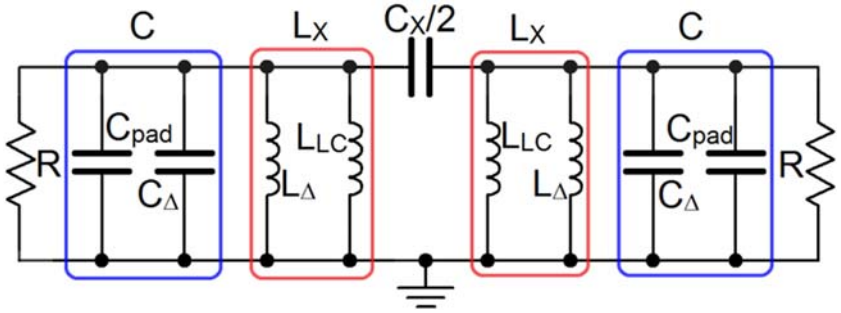


Fig. 8. Equivalent circuit of the filter circuitry in Fig. 4(b) at f_2.

Since the values of L_{Y1} and k_L in (11)-(12) are inter-dependent, the design procedure for the LC resonator employed in Fig. 4(b) requires iterative computation

and therefore is not as straightforward as that used for the λ/4 stub. To address this issue the following design method is proposed:

Step 1: Choose the values of R, C_{pad}, and R_I according to the system requirements.

Step 2: Consider the circuit in Fig. 8; this illustrates the equivalent circuit of the filter in Fig. 4(b) at f_2. Capacitance C in Fig. 2(a) is now represented by C_{pad} and C_Δ. L_X is comprised of L_{LC} and L_Δ. Set an initial value for C_Δ. For example: C_Δ is set equal to C_{pad}. As a result, $C = C_{pad} + C_\Delta = 2C_{pad}$.

Step 3: For given R, C (obtained from ***Step 2***) and R_I values, calculate L_X and C_X using (2) and (3) where ω refers to ω_2 i.e. the midpoint of the operating band.

Step 4: Compute α using (8).

Step 5: By assuming $k_L = k_C = 1$, calculate L_{Y1} and C_{Y1} using (11) and (10) respectively. This is done to ensure that the L_Y-C_Y tank circuit will provide a short circuit at f_1.

Step 6: Design and simulate a spiral inductor (L_Y) and a MIM capacitor (C_Y) such that their values at f_1 are equal to the values calculated in ***Step 5***. Subsequently determine the inductance and capacitance values at f_2 i.e. L_{Y2} and C_{Y2}.

Step 7: Using (14), calculate L_{LC} i.e. the equivalent net inductance of the L_{Y2}-C_{Y2} resonator tank at f_2.

$$Z_{LC}|_{\omega=\omega_2} = j\left(\omega_2 L_{Y2} - \frac{1}{\omega_2 C_{Y2}}\right) \leftrightarrow j\,\omega_2\,L_{LC}$$

$$\therefore\ L_{LC} = \frac{\omega_2^2 L_{Y2} C_{Y2} - 1}{\omega_2^2 C_{Y2}} \qquad (14)$$

Step 8: Given the values of L_X computed in ***Step 3*** and L_{LC} computed in ***Step 7*** the value of the excess inductance L_Δ can be determined as follows

$$L_{\Delta} = \frac{L_{LC}\, L_X}{L_{LC} - L_X} \qquad (15)$$

Step 9: C_Δ is employed to compensate for L_Δ, implying that L_Δ must resonate with C_Δ at f_2 so as to present an open circuit. Hence:

$$C_{\Delta} = \frac{1}{\omega_2^2 L_{\Delta}} \qquad (16)$$

Step 10: Compare the value of C_Δ calculated in ***Step 9*** with its initial value set in ***Step 2***. If their values are not equal, then go to ***Step 2*** and repeat the subsequent procedures.

For R = 50 Ω, R_I = 16 Ω and C_Δ initially set equal to C_{pad} resulting in $C = 2C_{pad}$ = 50 fF, the values of $C_X/2$ and L_X in Fig. 2(a) are respectively 42 fF and 35 pH, calculated using (2)-(3). In order to minimize capacitance variation of $C_X/2$ across the operating band this component was implemented using four 5 μm × 15 μm MIM capacitors connected in series instead of a single smaller capacitance, resulting in $C_X/2$ = 40 fF at 81 GHz and 44 fF at 86 GHz. The inductance L_Y and the capacitance C_Y in Fig. 4(b) are then calculated using (11) and (10), resulting in L_Y = 85 pH and C_Y = 75 fF (note that here f_1 is set to 63 GHz rather than 65 GHz as described in Section 2.2 with the aim to improve insertion loss at the lower end of the operating band, i.e., 81 GHz).

L_Y was realized on the M4 layer using an octagonal spiral inductor with trace width = 5 μm and inner diameter = 40 μm. The M2 layer is used as a ground for the spiral inductor's return current. The inductance value, ESR and quality factor of the spiral inductor L_Y simulated in SONNET are plotted versus frequency in Fig. 9, and their values at f_1 = 63 GHz and f_2 = 83.5 GHz are presented in Table III where k_L = 1.05. C_Y was realized using a 4 μm × 11 μm MIM capacitor. The capacitance value, ESR and quality factor of the MIM capacitor C_Y simulated in SONNET are plotted

versus frequency in Fig. 10, and their values at 63 GHz and 83.5 GHz are summarised in Table IV where $k_C = 1.12$.

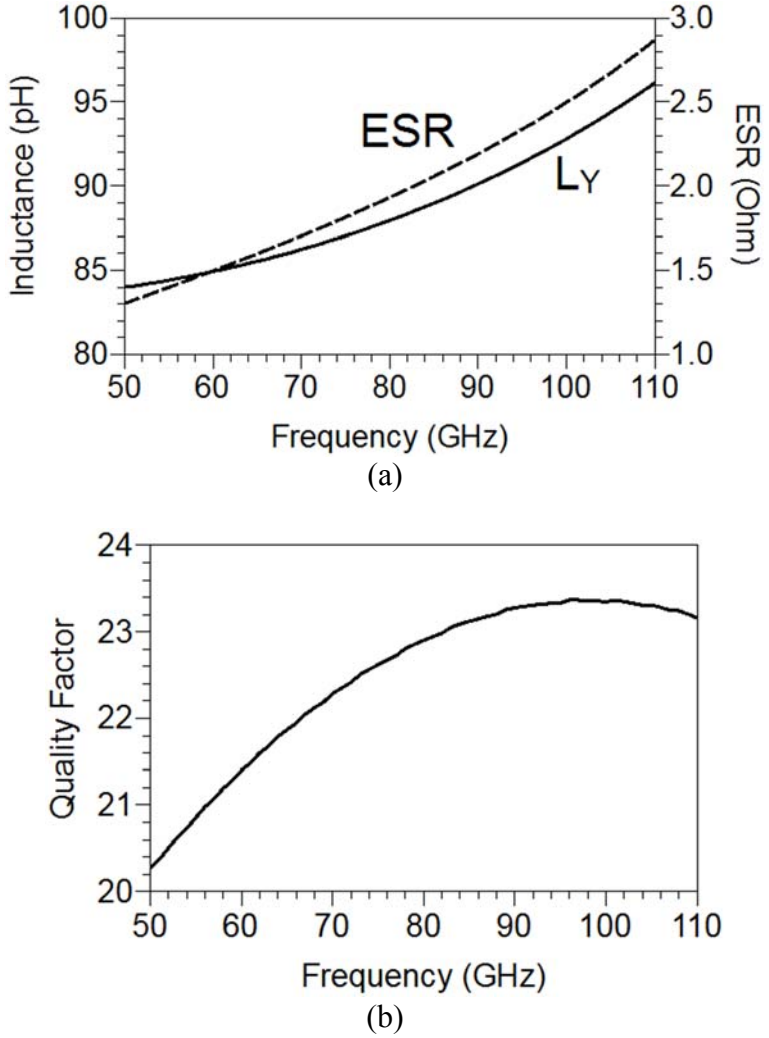
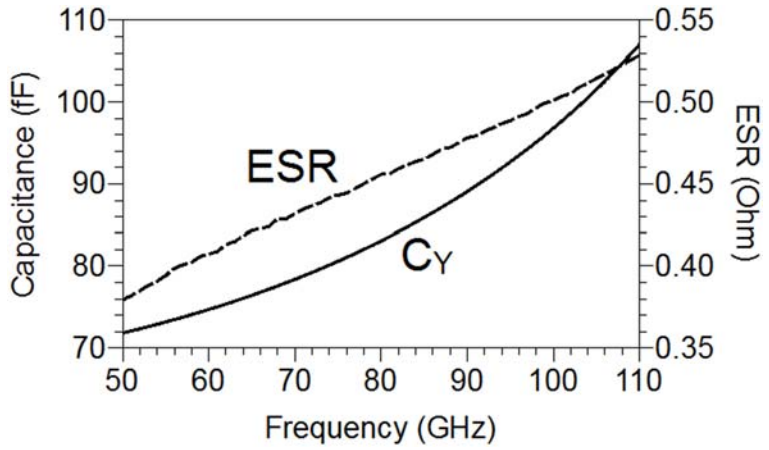


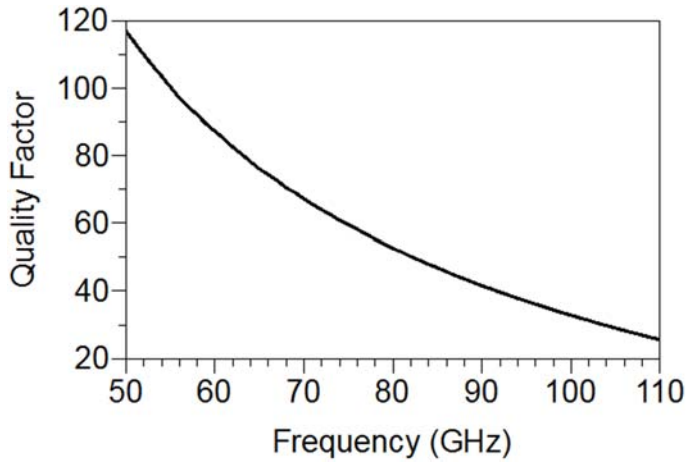
Fig. 9. (a) Inductance value, parasitic series resistance and (b) quality factor of the spiral inductor L_Y simulated in SONNET.

Table III. Inductance value, parasitic series resistance and quality factor of the spiral inductor L_Y simulated in SONNET

	63 GHz	83.5 GHz
Inductance (pH)	85	89
ESR (Ω)	1.6	2
Quality factor	22	23



(a)



(b)

Fig. 10. (a) Capacitance value, parasitic series resistance and (b) quality factor of the MIM capacitor C_Y simulated in SONNET.

Table IV. Capacitance value, parasitic series resistance and quality factor of the MIM capacitor C_Y simulated in SONNET

	63 GHz	83.5 GHz
Capacitance (fF)	76	85
ESR (Ω)	0.42	0.46
Quality factor	80.5	48

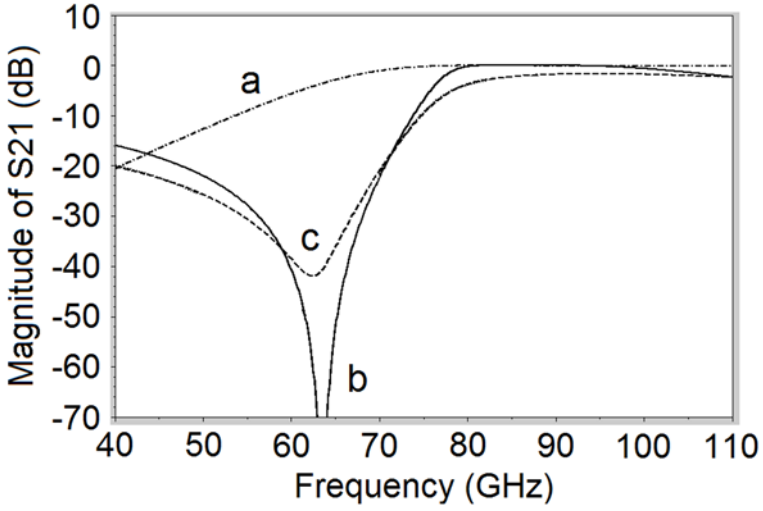
Using (14), L_{LC} in Fig. 8 can be obtained, i.e., L_{LC} = 47 pH. Subsequently L_Δ in Fig. 8 can be computed using (15), L_Δ = 137 pH. The value of C_Δ required to resonate with L_Δ is calculated using (16), C_Δ = 25 fF. Since this capacitance is equal to its initial value no further iteration is required. Illustrated in Fig. 5(b) is the layout of the LC

resonator filter. It measures 268 μm × 238 μm, consuming only half the chip die area of the λ/4 TL filter.

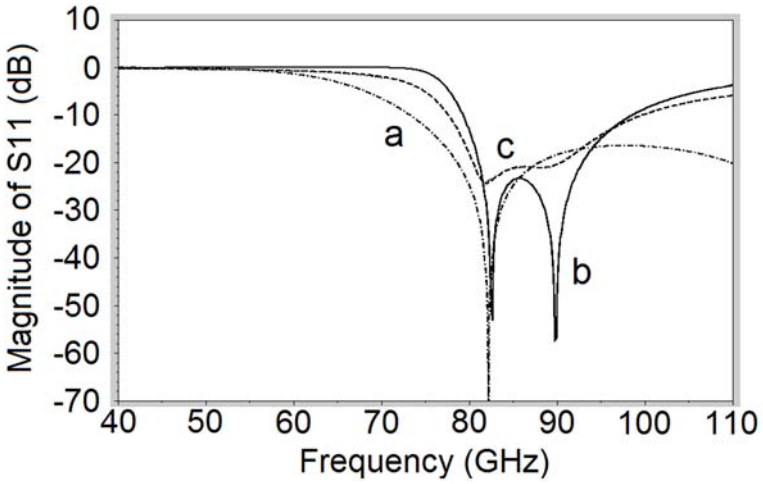
In the example above, frequency dispersion of L_Y and C_Y is relatively modest, i.e., $k_L = 1.05$ and $k_C = 1.12$. However, from Fig. 2(d), it can be observed that the value of L_X needs to be reduced by as large as 30% if the value of C is doubled from 25 fF (C_{pad}) to 50 fF ($2C_{pad}$). Therefore the frequency dispersion of passive lumped components must be carefully taken into account in the design.

3.3 Simulation Results

The third-order filter in Fig. 2(a) exhibits poor rejection level of around 5 dB at the image frequency. By employing λ/4 stubs, Fig. 4(a), the selectivity of the filter can be significantly improved. Simulated transmission loss ($|S_{12}|$ or $|S_{21}|$) and return loss ($|S_{11}|$ r $|S_{22}|$) of the λ/4-TL filter are shown in Fig. 11. Rejection levels higher than 30 dB are achieved from 54.4 GHz to 66.9 GHz with a -42 dB notch occurring at 62.5 GHz. Transmission losses within the operating band range between 2.1 and 3.25 dB. Return loss is better than 10 dB from 77.6 GHz to 99.8 GHz.



(a)



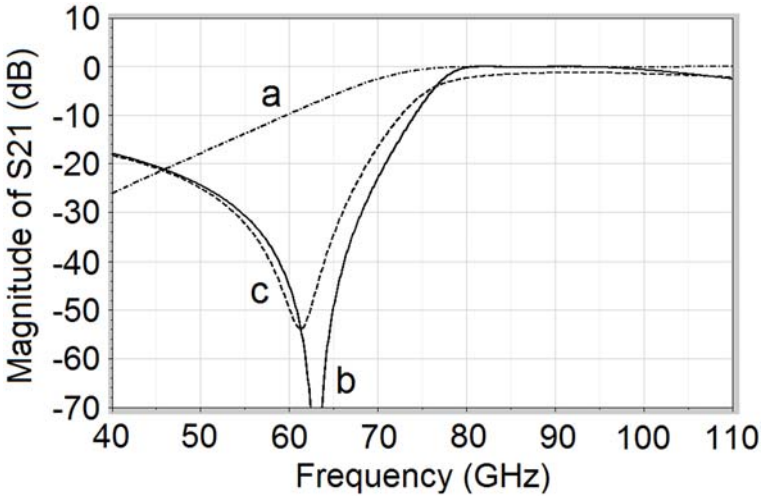
(b)

Fig. 11. (a) Insertion loss and (b) return loss of the λ/4 TL filter, simulated using ideal components (***curve b***) and using actual component models obtained from EM simulations (***curve c***). For comparison, the insertion loss and return loss of the filter in Fig. 2(a) simulated using ideal components (***curve a***) is also given.

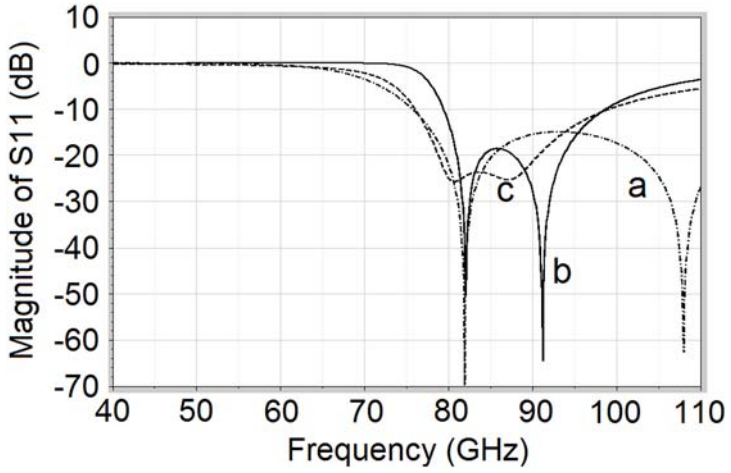
Simulated transmission loss and return loss of the series LC resonator filter in Fig. 4(b) wherein L_Y was implemented using a spiral inductor are depicted in Figs. 12(a)-(b). When compared with the filter in Fig. 2(a), the series-LC resonator employed in Fig. 4(b) is shown to be effective in improving rejection level at the image frequency. The circuit exhibits rejection levels higher than 30 dB from 53.7 GHz to 66 GHz with a -54 dB notch occurring at 61.3 GHz. Transmission losses across the operating band vary between 1.5 and 2.1 dB, which are better than those obtained using λ/4 stub (i.e. 2.1 – 3.25 dB). This is because parasitic series resistance of the spiral inductor is lower than that of the λ/4 stub (Tables II and III). Return loss is better than 10 dB from 76 GHz to 99.1 GHz.

Simulated transmission loss and return loss of the series LC resonator filter in Fig. 4(b) wherein L_Y was realised using a transmission line are depicted in Figs. 12(c)-(d). The circuit exhibits rejection levels higher than 30 dB from 55 GHz to 64 GHz with a -44 dB notch occurring at 60.5 GHz. Transmission losses within the operating band vary between 1.7 and 2.1 dB. Return loss is better than 10 dB from 71.4 GHz to 92.4

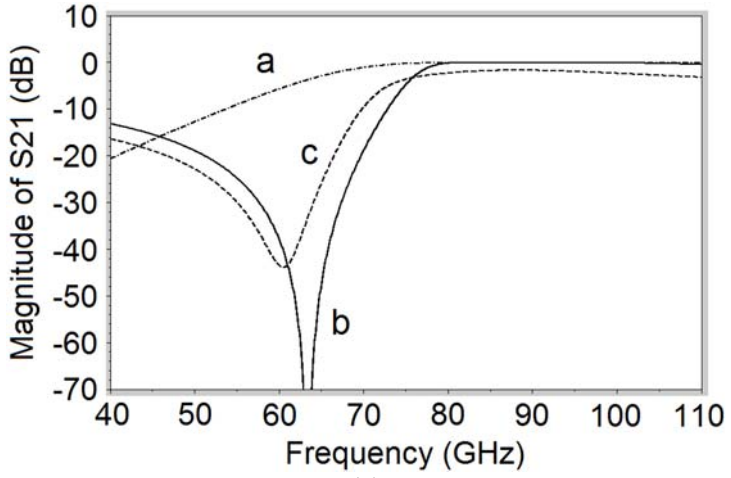
GHz.


Magnitude of S21 (dB)
10
0
-10
-20
-30
-40
-50
-60
-70
40
50
60
70
80
90
100
110
Frequency (GHz)
a
b
c

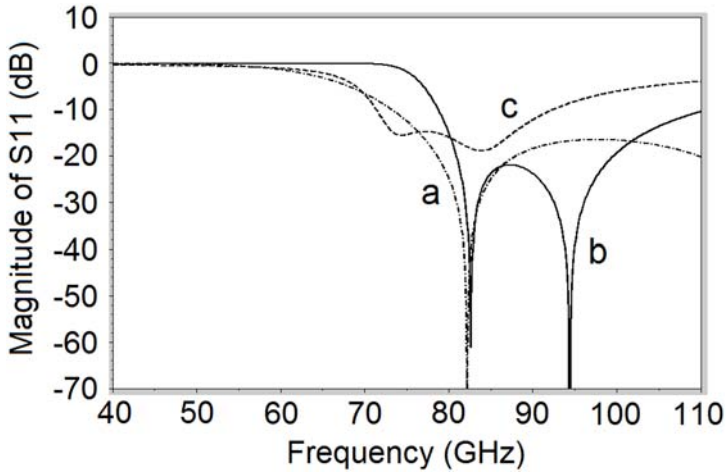
(a)


Magnitude of S11 (dB)
10
0
-10
-20
-30
-40
-50
-60
-70
40
50
60
70
80
90
100
110
Frequency (GHz)
a
b
c

(b)


Magnitude of S21 (dB)
10
0
-10
-20
-30
-40
-50
-60
-70
40
50
60
70
80
90
100
110
Frequency (GHz)
a
b
c

(c)



(d)

Fig. 12. (a) Insertion loss and (b) return loss of the LC-spiral filter, (c) insertion loss and (d) return loss of the LC-TL filter, simulated using ideal components (***curve b***) and using actual component models obtained from EM simulations (***curve c***). For comparison, the insertion loss and return loss of the filter in Fig. 2(a) simulated using ideal components (***curve a***) is also given.

4. Characterization

Three chip prototypes, Fig. 13, have been fabricated based on the λ/4 TL filter circuitry in Fig. 4(a) and the series LC resonator filter circuitry in Fig. 4(b) with L_Y realised either using a spiral inductor or a TL. Small-signal measurements were undertaken using an Agilent 110 GHz general-purpose network analyser (PNA) and Cascade GSG probes with 100 μm pitch.

Measured and simulated *S*-parameter results of the filters with λ/4 TL and series LC resonator are compared in Fig. 14 from which we can see that they are in reasonable agreement. From Fig. 14(a), it can be observed that the λ/4 TL filter exhibits higher than 30 dB rejection from 49.5 GHz to 66.5 GHz with a -46 dB notch at 58.3 GHz and transmission loss ranging from 3.6 dB to 5.2 dB across the operating band. Measured return loss was better than 10 dB within a frequency range 80-102 GHz. The filter that employs a series LC spiral network results in rejection greater than 30 dB from 54 GHz to 67 GHz with a -46 dB notch occurring at 60.5 GHz, Fig. 14(b). Measured

transmission loss varied between 3.1 dB and 4.7 dB across the operating band and return loss higher than 10 dB was obtained over a wide frequency range 80-110 GHz. From Fig. 14(c), it can be observed that the LC-TL filter exhibits 3.6-5.0 dB insertion loss across the operating band. Higher insertion losses observed in the measurements could be due to the presence of stronger parasitic capacitive coupling to the low-resistivity substrate than simulated. The measured *S*-parameters and group delay of all three filter prototypes are plotted and compared in Fig. 15. The performances of the filters reported in this paper are summarized and compared with other published mm-wave filters in Table V.

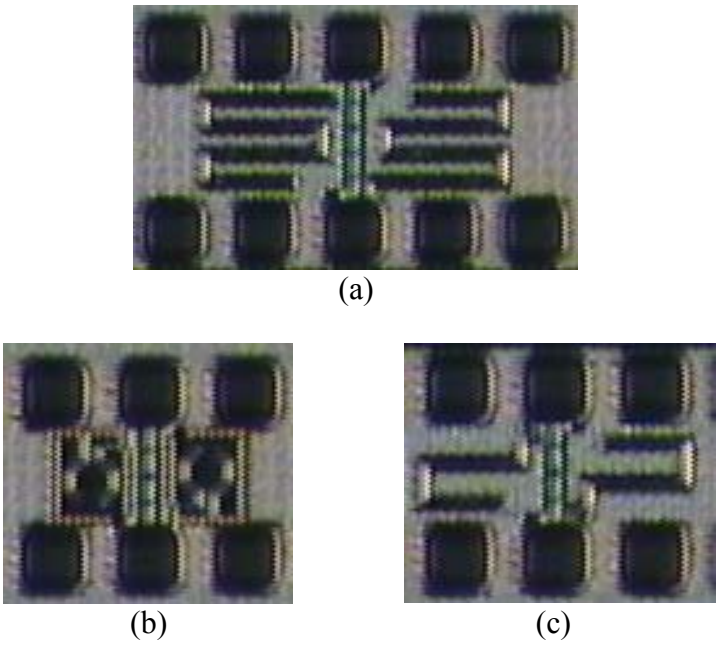
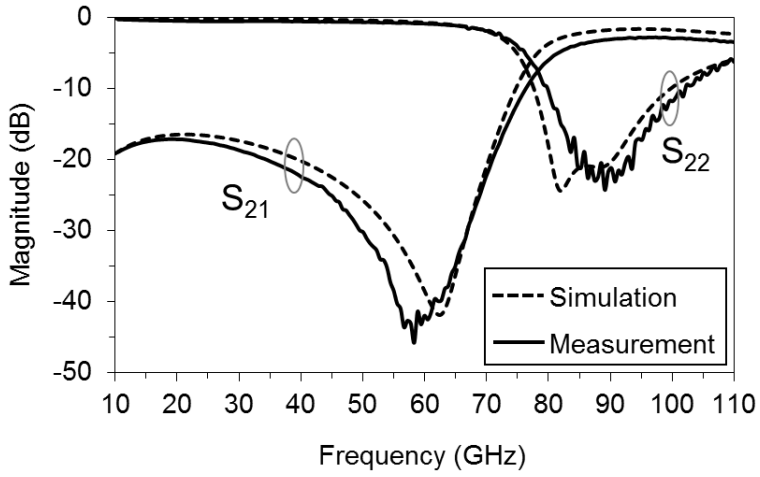
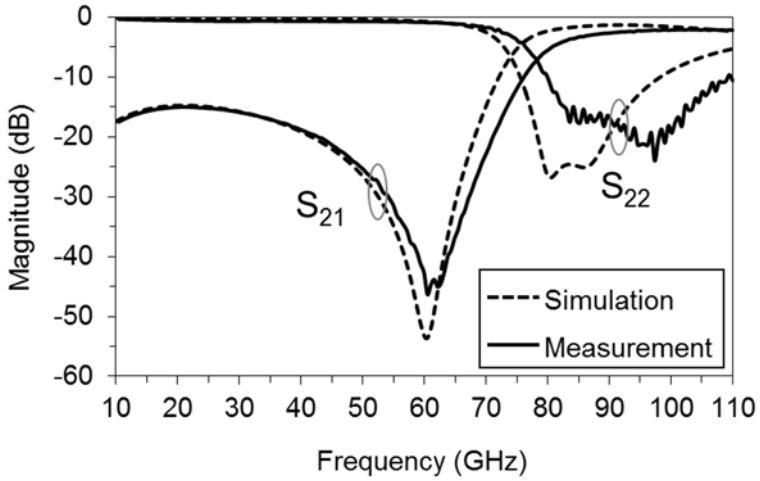


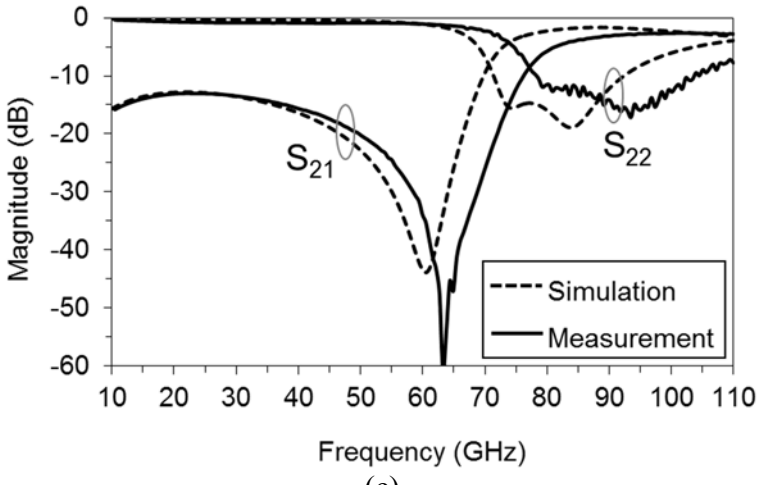
Fig. 13. Chip microphotographs of image-reject filters: (a) using λ/4 lines measured 468 μm × 266 μm, (b) using LC-spiral inductor measured 268 μm × 238 μm, and (c) using LC-TL measured 332 μm × 238 μm.



(a)



(b)



(c)

Fig. 14. Measured vs simulated *S*-parameters: (a) λ/4 filter, (b) LC-spiral filter, and (c) LC-TL filter.

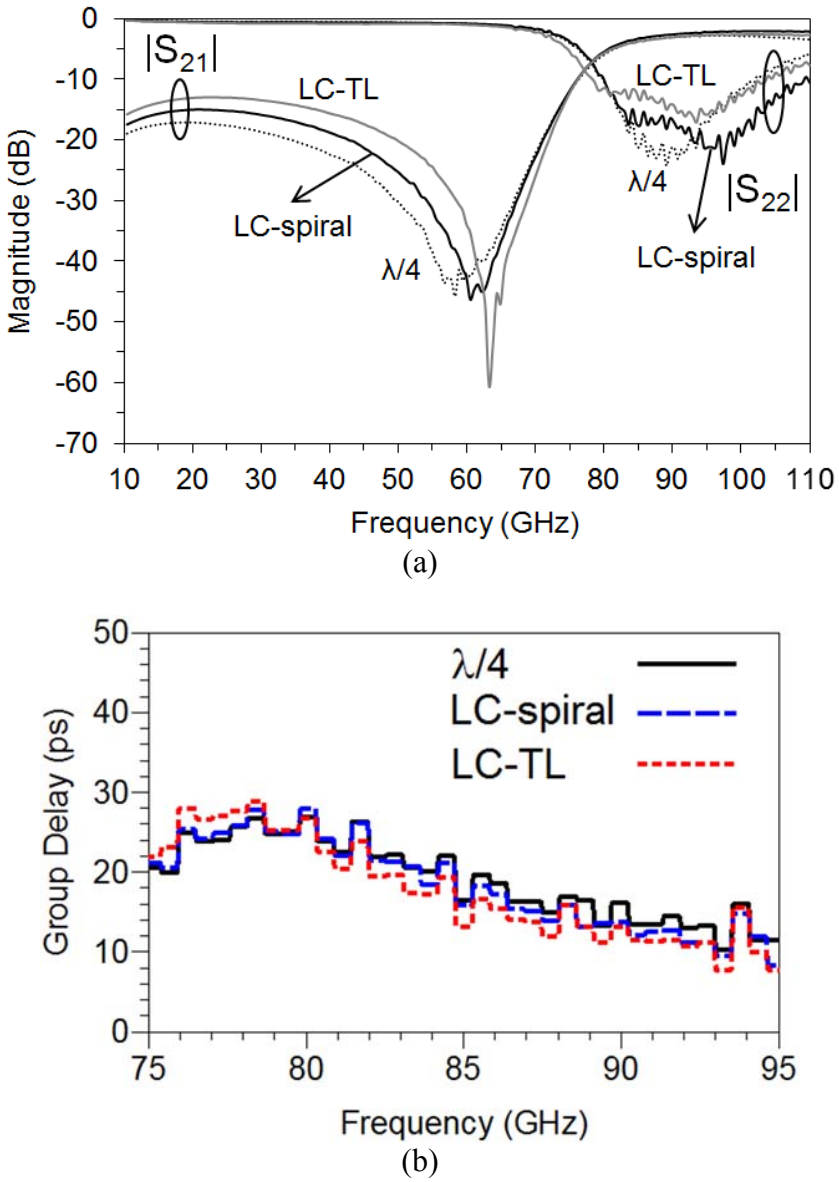


Fig. 15. (a) Measured *S*-parameters and (b) group delay of the λ/4, *LC*-spiral, and *LC*-TL filters.

Table V. Performance Comparison with Other Millimetre-Wave On-Chip Filters

Ref	Process	Frequency (GHz)	Insertion Loss (dB)	Attenuation Slope (dB/10 GHz)	Area (mm^2)
[7]	GaAs	31.3-45	<2.7	40	1.5
[8]	CMOS	50.8-56	>5.5	30/14	0.087
[11]	CMOS	44.5-75.5	>3.9	4/4	0.85
[12]	CMOS	77	9.3	11/9	0.11
[13]	SiGe	71.3-83.3	6.4-9.4	20.5/12	0.107
[14]	SiGe	50.5-66	4-6	16/6	0.185
Fig.13(a)	SiGe	81-86	3.6-5.2	23.4	0.125
Fig.13(b)	SiGe	81-86	3.1-4.7	25.6	0.064
Fig.13(c)	SiGe	81-86	3.6-5.0	27.7	0.079

5. Conclusion

A simple yet effective third-order high-pass filter topology is proposed to address the detrimental effects of parasitic pad capacitances on the filter performance at mm-wave frequencies. By incorporating this parasitic capacitance into the filter circuit, the chips characterisation procedures can be simplified, i.e., no de-embedding process required. Importantly, an intermediate resistance (R_I) is introduced in the analysis and investigation as to how this parameter affects the rejection level across the image band and the bandwidth of the passband has been undertaken. Small R_I values result in high rejection level but narrow band matching. Further, an iterative design method is proposed to address the issue of the frequency dispersion of the inductance and capacitance of the lumped reactive components employed in the filter circuits. In order to validate the filter synthesis and design methodologies described in this paper three filter prototypes have been designed, fabricated and measured. Transmission zeroes are created by means of a quarter-wave transmission line (filter 1) and a series LC resonator (filters 2 and 3). Measured transmission losses across the operating band are 3.6-5.2 dB (filter 1), 3.1-4.7 dB (filter 2), and 3.6-5.0 dB (filter 3). Measured attenuation slopes of these filters are respectively 23.4, 25.6, and 27.7 dB per 10 GHz and when compared with other reported filters represent best in class operation.

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